

CHARACTERIZATION OF THE OXIDE-SEMICONDUCTOR INTERFACE IN NO, P, AND N-PLASMA PASSIVATED 4H-SiC/SiO₂ STRUCTURES USING TEM AND XPS

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2013 Fall MRS Meeting - T8.04
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Motivation and background

- SiC: Very promising for MOS devices in high temperature, high power, and high radiation environments
 - MOSFET devices limited by poor channel carrier mobility and reliability
 - Best device μ_{FE} : SiC $\sim 125 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ (a-face P passivation)[◇]; Si $\sim 600 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ (uniaxial <100> strain)[◇]
 - Electrically active defects at the SiC/SiO₂ interface inhibit devices during channel inversion
 - Interfacial roughness/unique bonding states
- How to passivate these defects and improve mobility?
 - Incorporation of N at interface
 - NO anneal – improves μ , but can introduce additional defects[†]
 - N-plasma anneal – incorporates N without additional oxidation[⊖]
 - Incorporation of P at interface
 - Anneal in P₂O₅ – P dopants have lower activation energy than N[⊗]
 - N and P passivate dangling bonds/modify interface

[◇]G. Liu *et al.*, IEEE Electron. Dev. Lett. **34**, 181–183 (2013).

[⊖]X. Zhu *et al.*, Solid-State Electron. **57**, 76–79 (2011).

[◇]K. Uchida *et al.*, IEDM Tech. Dig. 229-232 (2004).

[⊗]Y. Sharma *et al.*, Solid-State Electron. **68**, 103–107 (2012).

[†]J. Rozen, in *Physics and Technology of Silicon Carbide Devices* (InTech, 2012), pp. 251–278.

Central questions

How do the structure and chemistry of the transition layer at the 4H-SiC/SiO₂ interface change under various processing conditions?

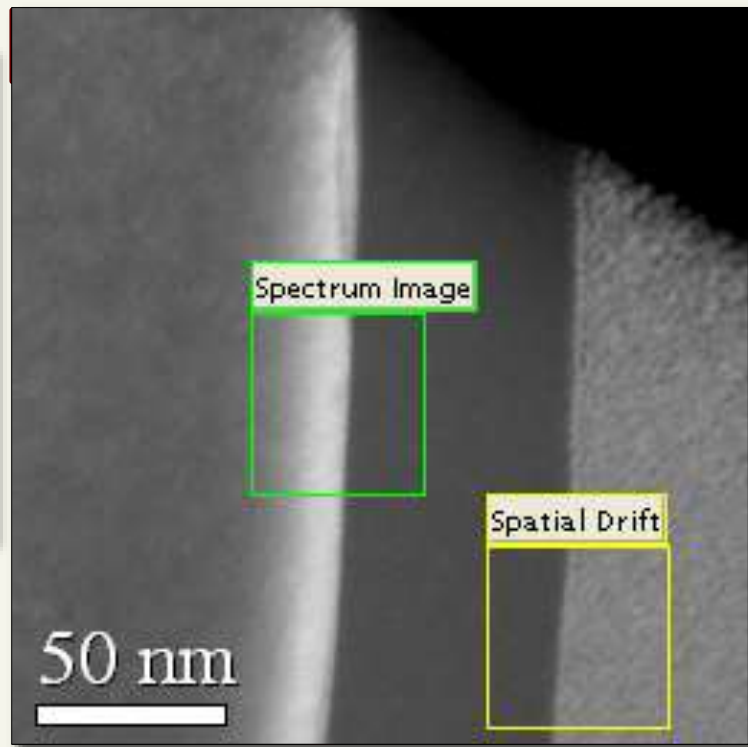
What do these changes tell us about the effects of these passivation processes?

Outline

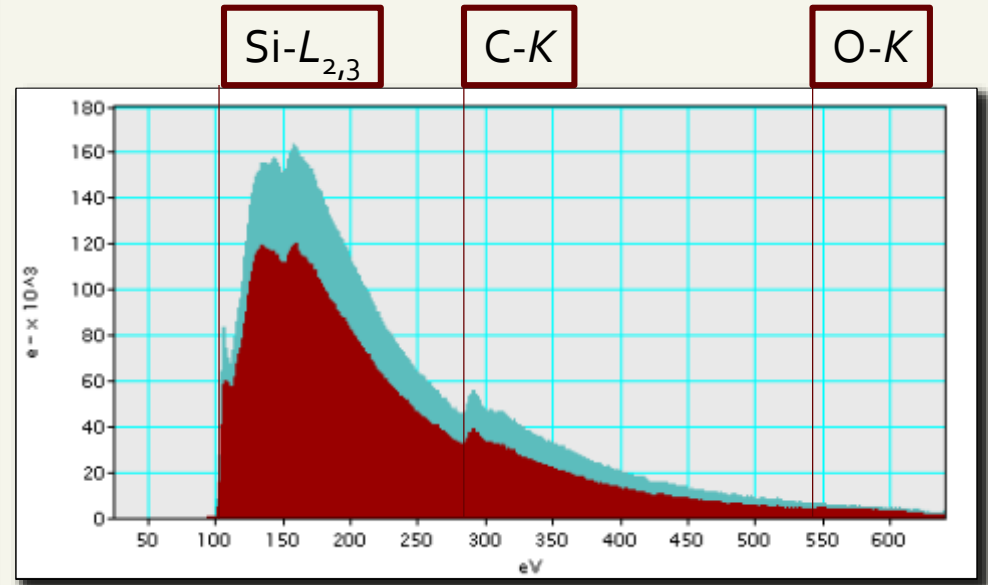
- Background/Review of prior work and methods
 - Characterization of transition layer in NO-annealed $4H$ -SiC MOSFETs
 - J. Taillon *et al.*, *J. Appl. Phys.* 113, 044517 (2013).
 - Transition layer width compared to electronic properties
- Recent work
 - Comparison of NO-annealed samples with P and N-plasma passivated $4H$ -SiC devices
 - Ongoing XPS experiments

BACKGROUND/PRIOR WORK

EELS Spectrum imaging

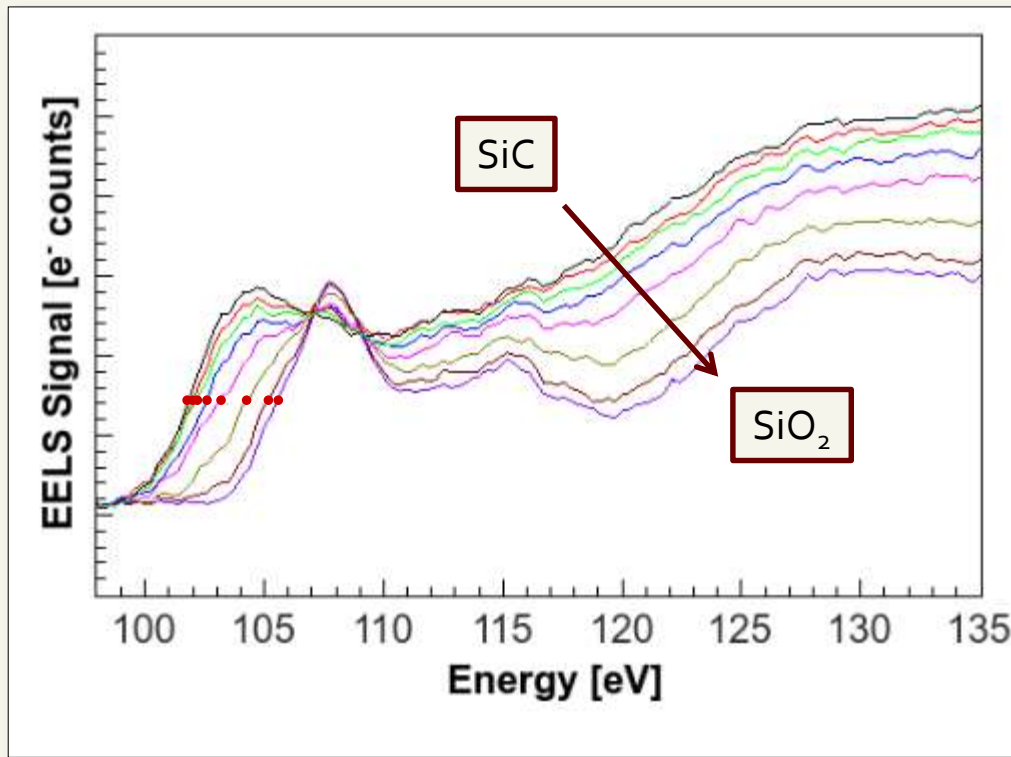


HAADF Image
(60 minute NO anneal)



Background-subtracted spectrum
(60 minute NO anneal)

Si- $L_{2,3}$ chemical shift

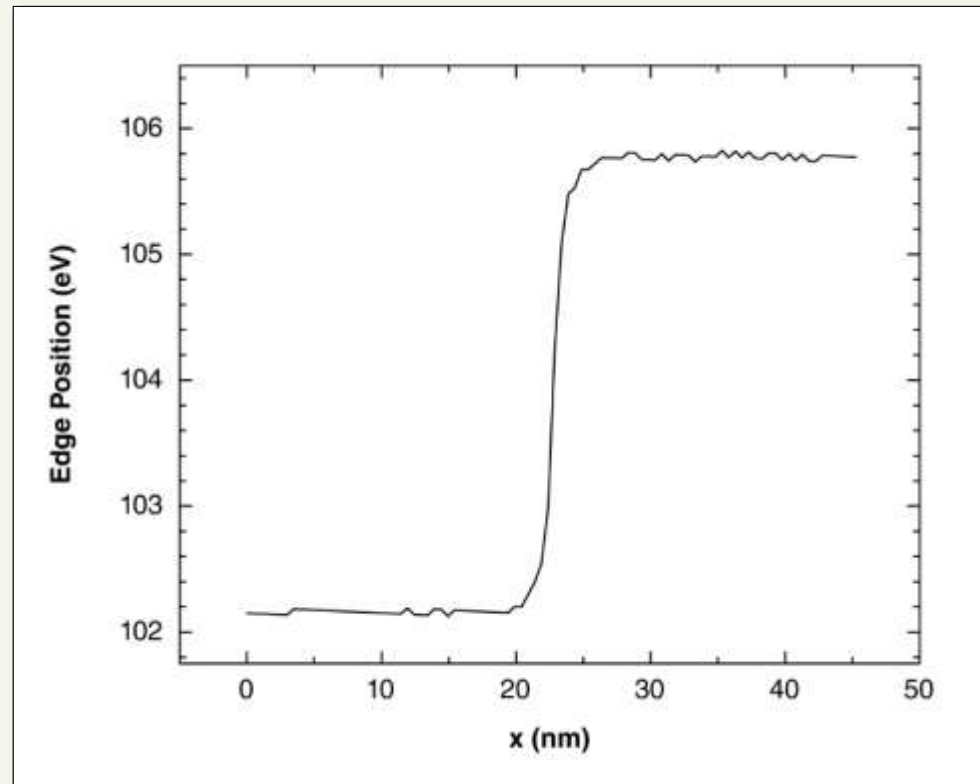


- EELS fine structure (ELNES) reflects local unoccupied density of states
 - Semiconductor → insulator
 - Edge onset → minimum energy needed to excite core shell e⁻
 - Band gap widens, core levels depressed relative to E_F ¹
 - Charge transfer from Si → C/O
 - Onset shifts to higher energy

¹ D. Muller, Ultramicroscopy **78**, 163 (1999).

Si- $L_{2,3}$ chemical shift

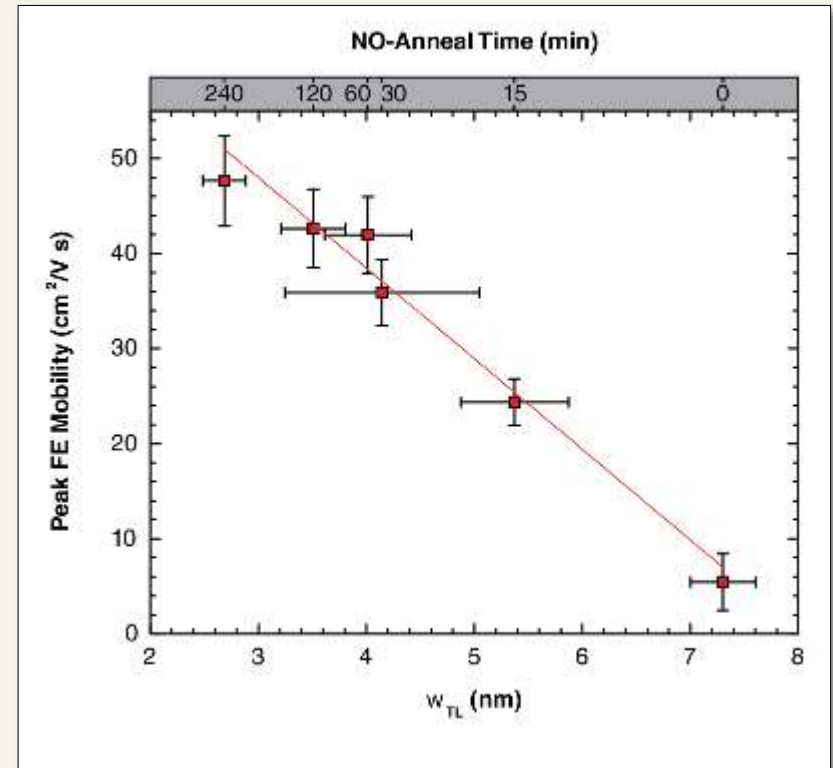
- Track inflection point of edge onset across interface¹
- Gradual and monotonic shift
 - Si bonding changes gradually and uniformly across the interface
- Measure extent of transition region (w_{TL}) as “rise time” of step



¹ D. Muller, P. Batson, and J. Silcox, Physical Review B **58**, 11970 (1998).

NO-anneal results

- 6 SiC/SiO₂ samples: 0-240 minutes of NO-anneal
- w_{TL} correlates inverse-linearly μ_{FE}
- NO-anneal removes/passivates mobility-limiting defects
 - Compositionally and electronically
- **Conclusions:**
 - w_{TL} decreases with increasing NO anneal time
 - New chemical shift of Si- $L_{2,3}$ edge onset was most reliable method



J. Taillon, L. Salamanca-Riba, *et al.*, *J. Appl. Phys.* 113, 044517 (2013).

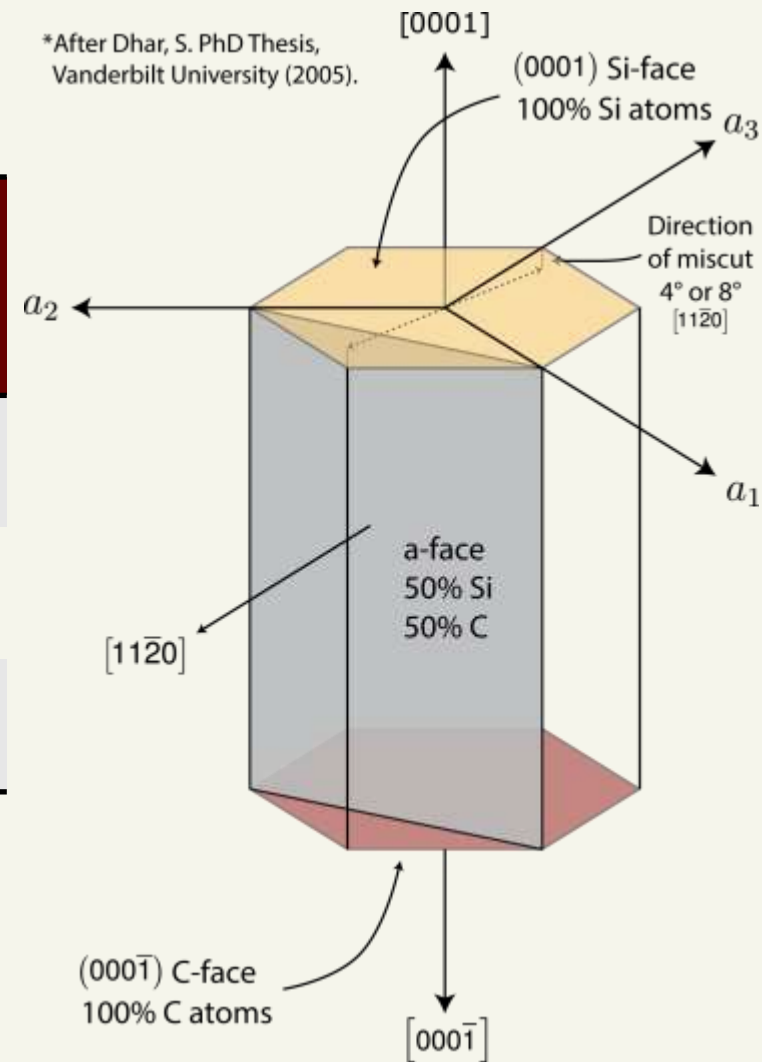
RECENT WORK

Recent work

Process \ Face	NO	P	N ₂ P
Si - (0001)	2 hrs	4 hrs	2, 4, 6 hrs
a - (11 $\bar{2}$ 0)	2 hrs	4 hrs	X
C - (000 $\bar{1}$)	2 hrs	X	X

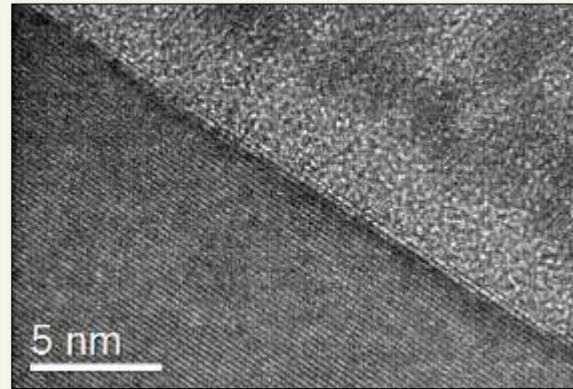
Miscut on Si and C faces:
4° or 8°

No miscut on *a* face



NO anneal

- Identical w_{TL} regardless of device face
 - All samples annealed for 2 hours
- Another aspect to mobility, besides w_{TL}
- Roughness of C-face sample does not seem to have large effect
 - *a*-face?

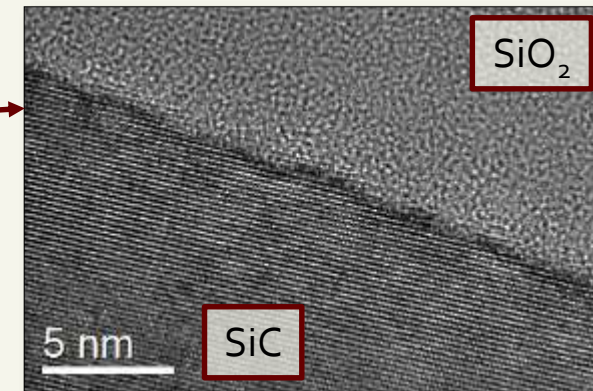


■ Si face

4° miscut evident
Thin oxide layer

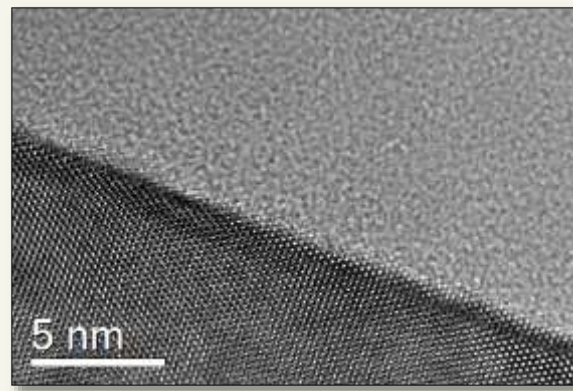
● C face

8° miscut
Greater roughness



SiO₂

SiC



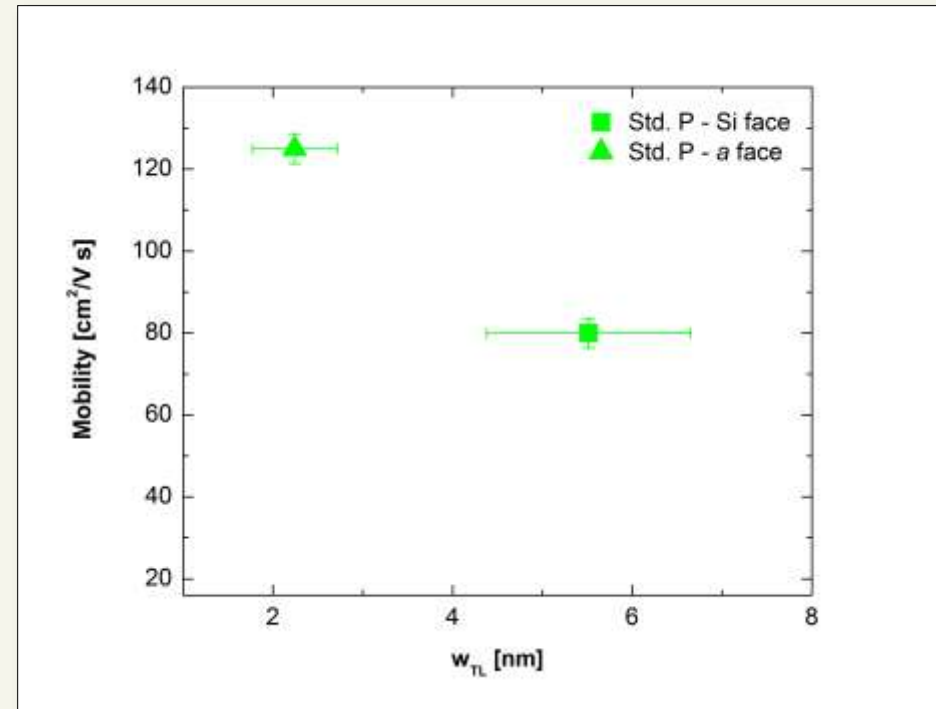
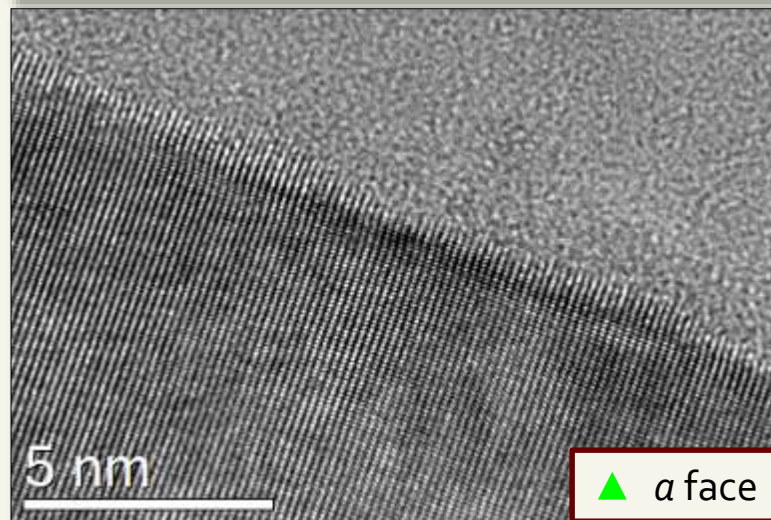
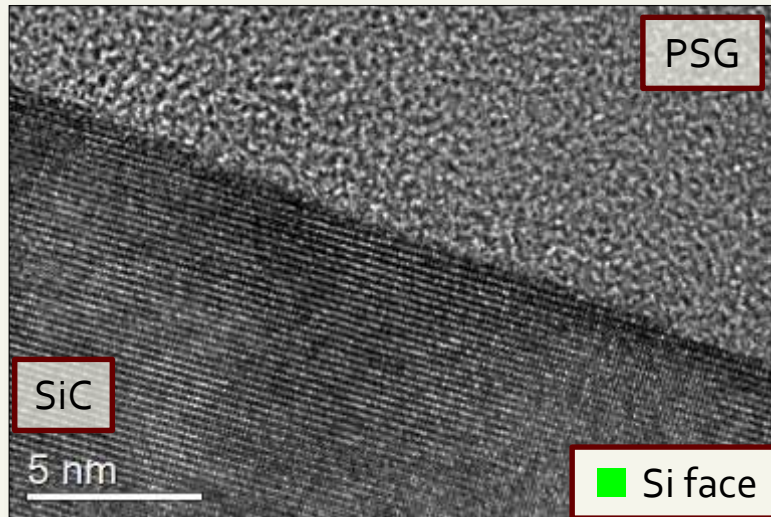
▲ *a* face

No miscut
Least roughness

Recent work

Device Process Crystal face	NO	P	N ₂ P
Si - (0001)	2 hrs	4 hrs	2, 4, 6 hrs
a - (11 $\bar{2}$ 0)	2 hrs	4 hrs	X
c - (000 $\bar{1}$)	2 hrs	X	X

P anneal

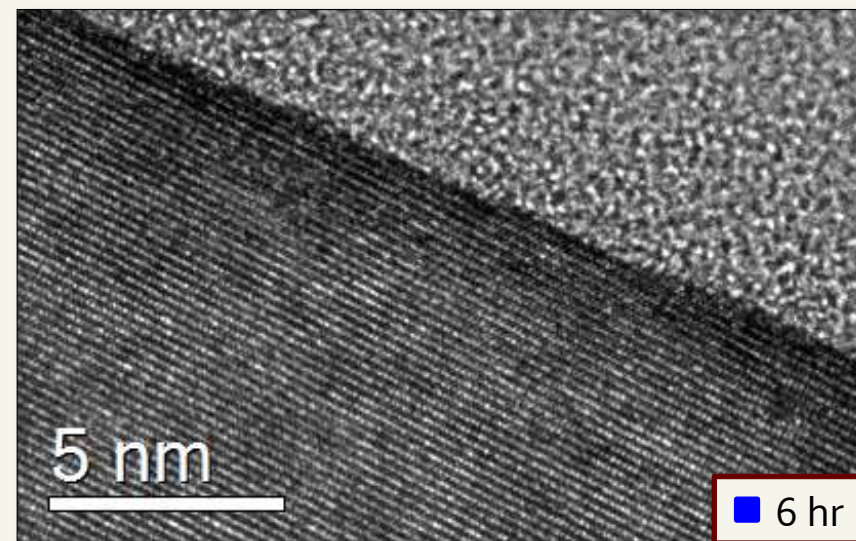
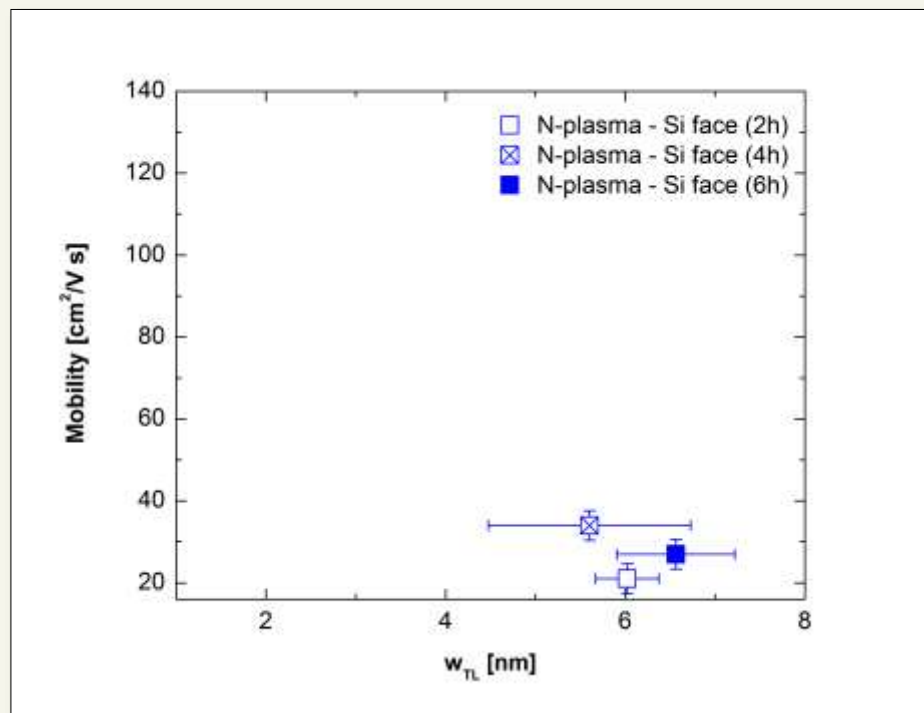


- HRTEM images similar to NO-anneal counterparts
- Much higher mobilities, w_{TL} "trend"

Recent work

Device Process Crystal face	NO	P	N ₂ P
Si - (0001)	2 hrs	4 hrs	2, 4, 6 hrs
a - (11 $\bar{2}$ 0)	2 hrs	4 hrs	X
c - (000 $\bar{1}$)	2 hrs	X	X

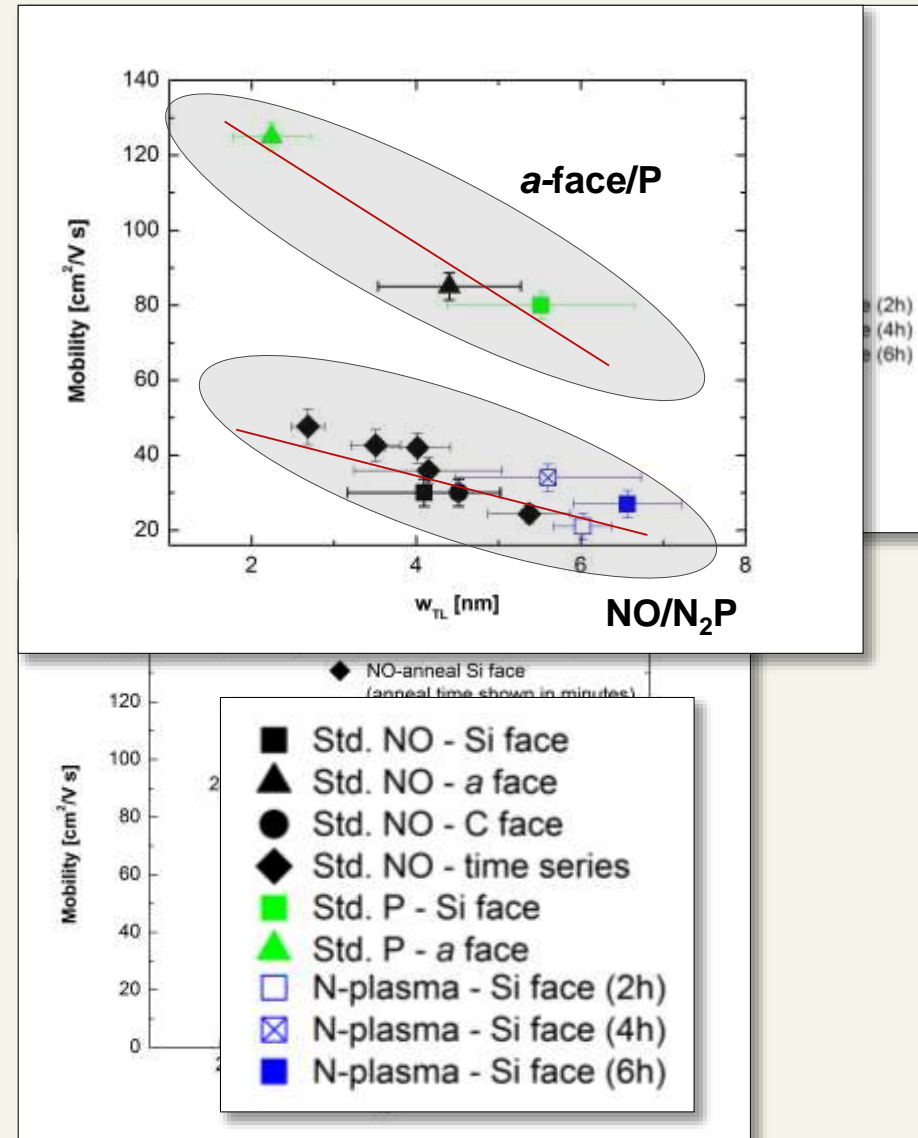
N₂P anneal



- Chemical shift measurements reveal larger w_{TL} that agree with low μ

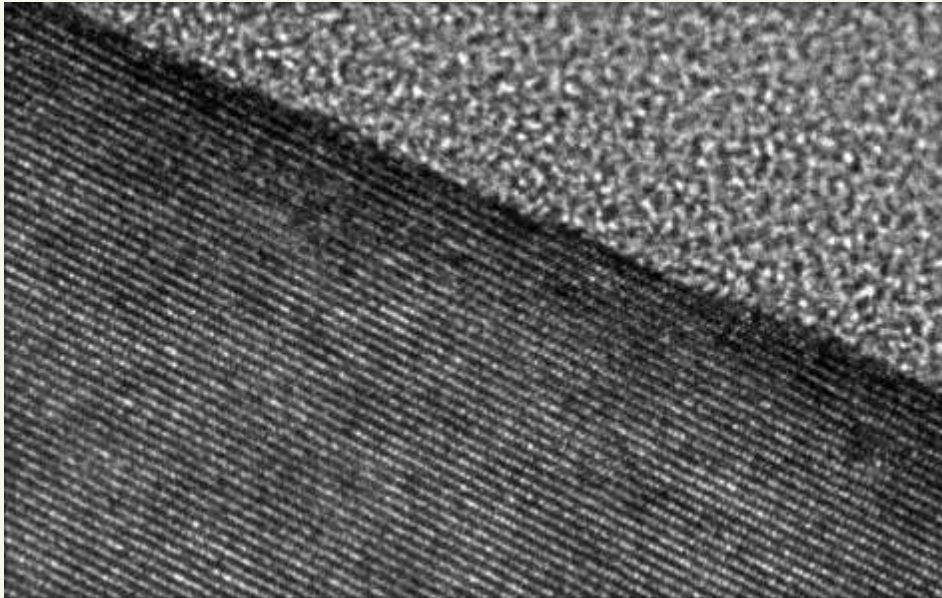
TL Conclusions

- NO, P, & N-plasma samples:
 - Large variation in μ and w_{TL}
 - Less obvious trend than NO annealed samples alone
 - α -face and P-anneal samples have higher μ
 - Higher roughness does not guarantee larger w_{TL} (when considering C-face sample)
- Seem to have two distinct regimes, with similar but distinct relationships
 - More data needed to confirm this
- Need to investigate fine structure in more detail to gain additional insight



ONGOING WORK

Further HRTEM analysis



$$G(\mathbf{u}) = T(\mathbf{u})F(\mathbf{u})$$

$$G(\mathbf{u}) = A(\mathbf{u})E(\mathbf{u})2 \sin \chi(\mathbf{u}) F(\mathbf{u})$$

$$\chi(u, \Delta f) = \pi(\Delta f)\lambda u^2 + \frac{1}{2}\pi C_s \lambda^3 u^4$$

- Roughness can be used to calculate power spectrum
 - Estimation of surface scattering-limited μ possible from this ^{1,2}
- How to measure?
 - Difficult to digitize based on single image
 - HRTEM focal series reconstruction \rightarrow complex wave function
 - Comparison with multislice simulations (QSTEM)³
- Geometric Phase Analysis (GPA)
 - Strain mapping at interface

¹ Goodnick, S., *et al.*, Physical Review B, **32**, 8171–8186 (1985).

² Zhao, Y., *et al.*, IEEE Electron Device Letters, **30**, 987–989 (2009).

³ <http://www.qstem.org>

XPS depth profiles

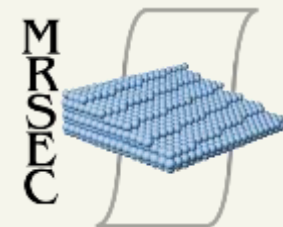
- Well-controlled chemical depth profile
- Motivation:
 - Suboxide states observed near SiC in slow oxide growth
 - Compare Si $2p$ and C $1s$ transition states in XPS to Si- $L_{2,3}$ and C- K EELS
- “Spin-etch” depth profile to investigate native oxide of SiC in NO-annealed devices
 - Technique developed by Grunthaner *et al.* to investigate Si/SiO₂



¹ Grunthaner, F. J. *et al.*, Journal of Vacuum Science and Technology, **16**, 1443 (1979)

Acknowledgements

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THANK YOU

Questions and comments?