CHARACTERIZATION OF THE OXIDE-SEMICONDUCTOR INTERFACE IN *4H*-SiC/SiO_2 STRUCTURES USING TEM AND XPS*

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Motivation and background

- SiC: Very promising for high temperature, high power, and high radiation environments
  - MOSFET devices limited by poor channel carrier mobility and reliability
  - Best device μ_{FE}: SiC ~ 125 $\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ (a-face P passivation)[1]; Si ~ 600 $\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}$ (uniaxial <100> strain)[2]
  - Electrically active defects at the SiC/SiO_2 interface inhibit devices during channel inversion
  - Other defects significantly affect the reliability and stability of devices over time
- What is the true nature of the interface, and how do our processing techniques really affect it?
  - EELS experiments suggest distinct transition region[2]
  - Other results (XPS, MEIS, etc.) suggest more abrupt transition [3 – 6]
  - What is NO post oxidation annealing really changing about the interface structurally and chemically?

[1] G. Liu *et al.*, IEEE Electron. Dev. Lett. **34**, 181–183 (2013).
[2] K. Uchida *et al.*, IEDM Tech. Dig. 229-232 (2004).
[3] J. Taillon, L. Salamanca-Riba, *et al.*, J. Appl. Phys. 113, 044517 (2013).
[4] H. Watanabe, *et al.*, Appl. Phys. Lett., 99(2), 021907 (2011).
[5] P. Tanner, *et al.*, J. Electron. Mater., 28(2), 109 (1999).
[5] P. Jamet, *et al.*, J. Appl. Phys., 90(10), 5058 (2001).
[6] X. Zhu, *et al.*, Appl. Phys. Lett., 97(7), 071908 (2010).

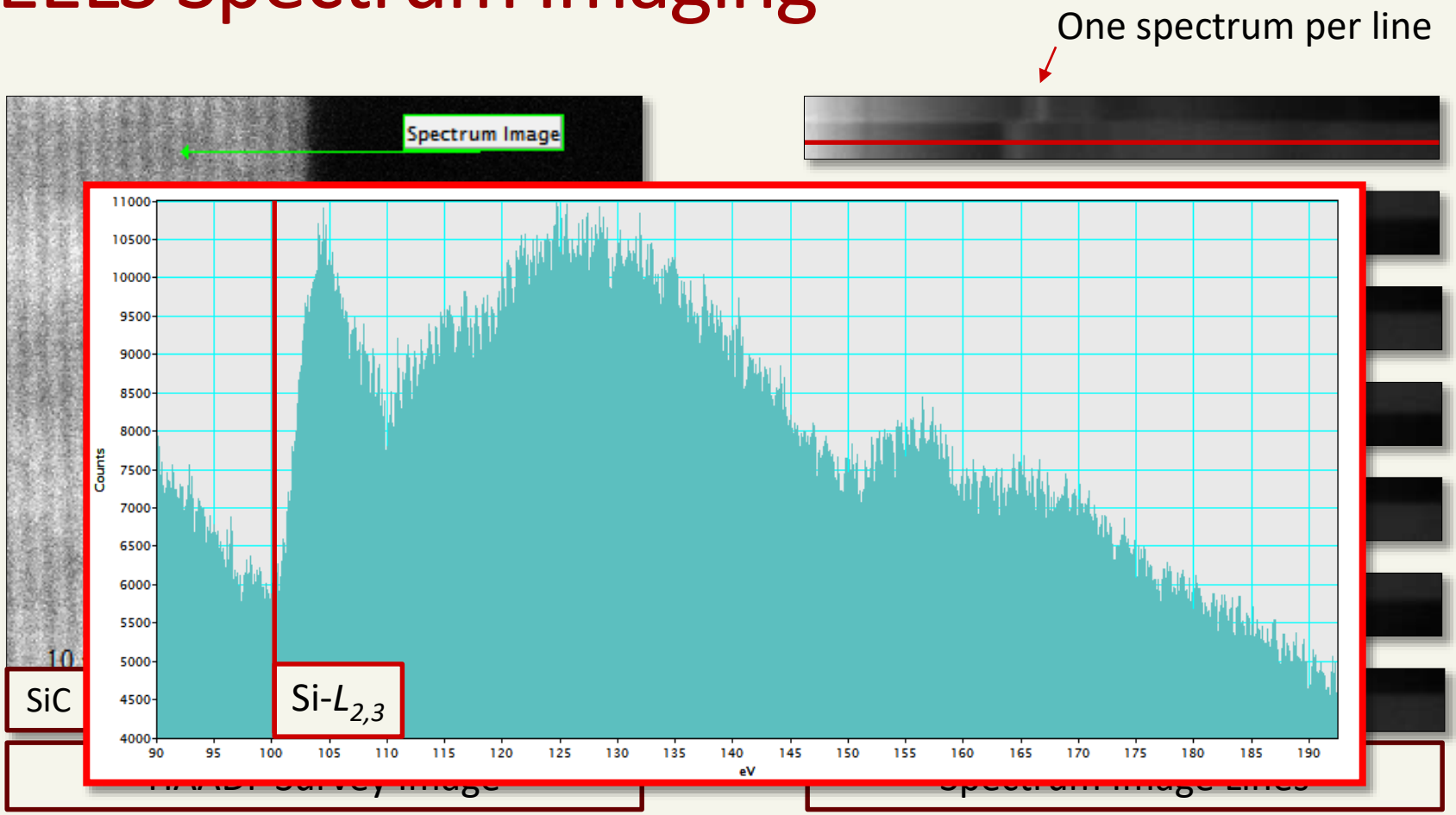
Outline

- TEM-EELS from on-axis and miscut samples
  - Analysis of oxidized and post oxidized NO annealed samples with various crystallographic orientations and annealing times.

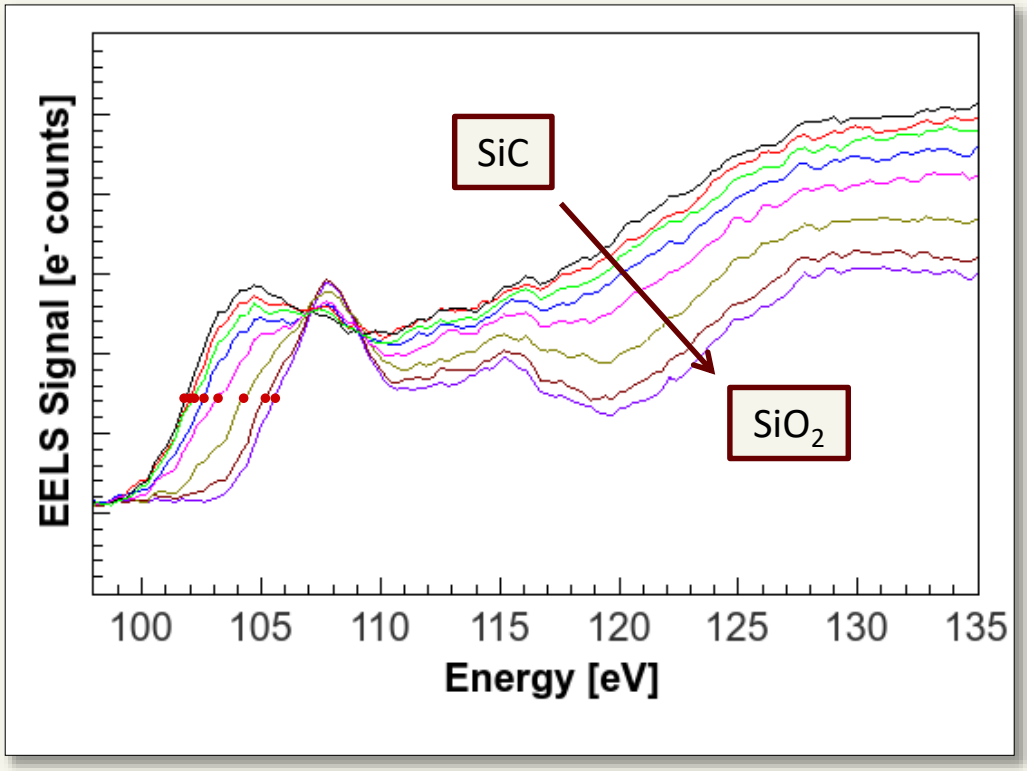
- Depth profiles and XPS
  - Development and refinement of SiO_2 spin-etch technique
  - XPS depth profiles

TEM-EELS EXPERIMENTS

EELS Spectrum Imaging



Si-$L_{2,3}$ chemical shift

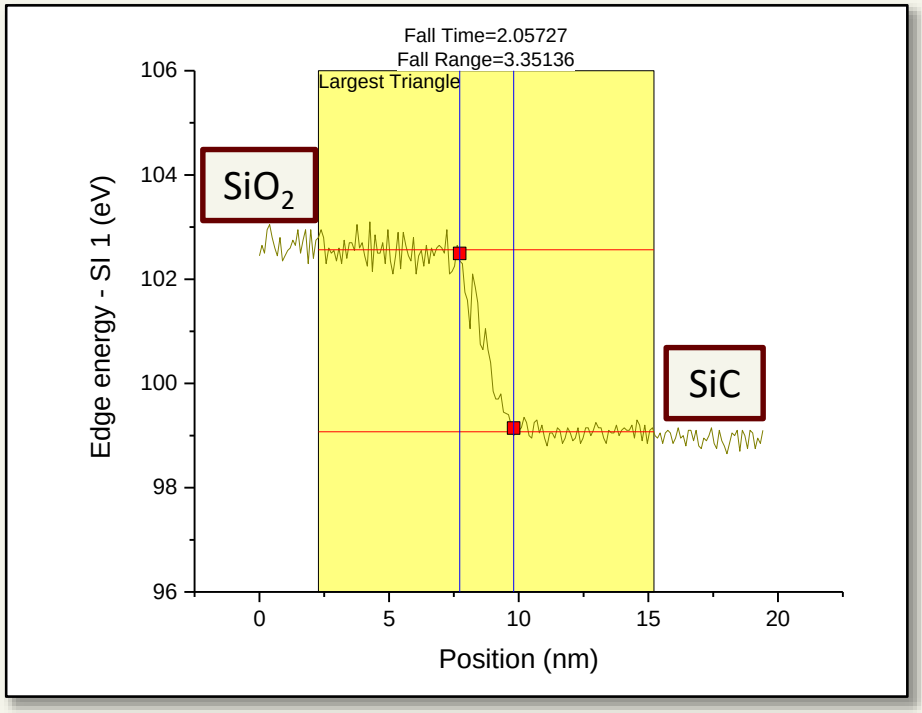


- EELS fine structure (ELNES) reflects local unoccupied density of states
  - Semiconductor → insulator
  - Edge onset → minimum energy needed to excite core shell e^-
  - Band gap widens, core levels depressed relative to E_F[1]
    - Charge transfer from Si → C/O
    - Onset shifts to higher energy

[1] D. Muller, Ultramicroscopy **78**, 163 (1999).

Si-$L_{2,3}$ chemical shift

- Track inflection point of edge onset across interface[1]
- Gradual and monotonic shift
  - Si bonding changes gradually and uniformly across the interface
- Measured using rise/fall time calculations typical in signal processing

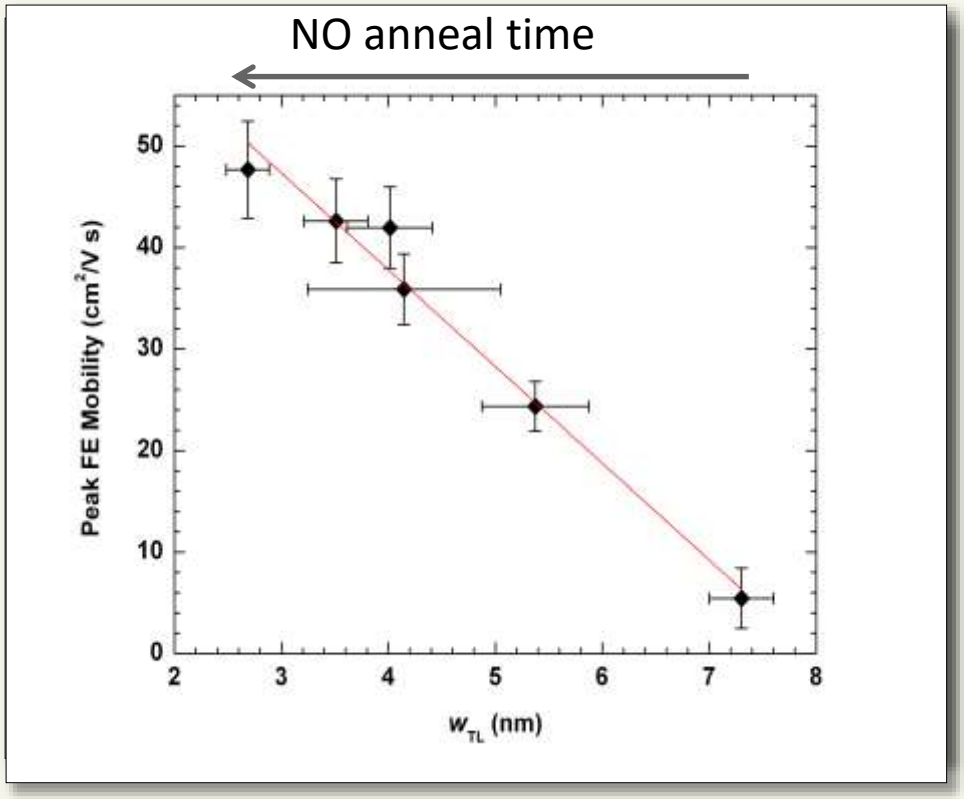


Example from new sample Si-O_2-0

[1] D. Muller, P. Batson, and J. Silcox, Physical Review B **58**, 11970 (1998).

NO-anneal results (previous results)

- w_{TL} correlates inverse-linearly μ_{FE}
  - Also correlates with decreased trap density: John Rozen, *et al*. IEEE Trans. Elec. Dev. (2011).
- NO-anneal removes/passivates mobility-limiting defects
  - Compositionally and electronically
- **Conclusions:**
  - w_{TL} decreases with increasing NO anneal time
    - New chemical shift of Si-$L_{2,3}$ edge onset was most reliable method
    - No excess C on either side of interface

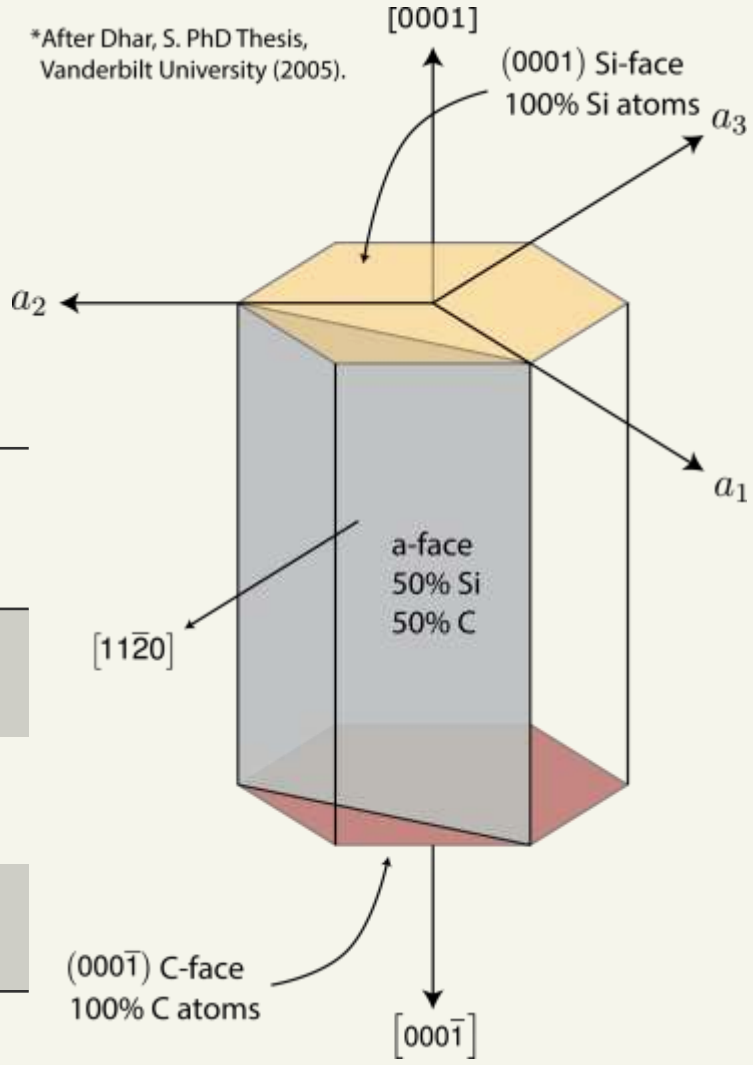


J. Taillon, L. Salamanca-Riba, *et al.*, *J. Appl. Phys.* 113, 044517 (2013).

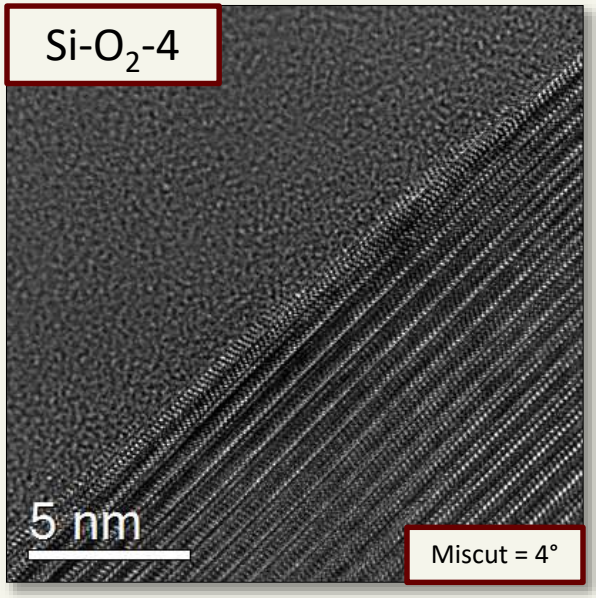
Samples investigated – TEM/EELS

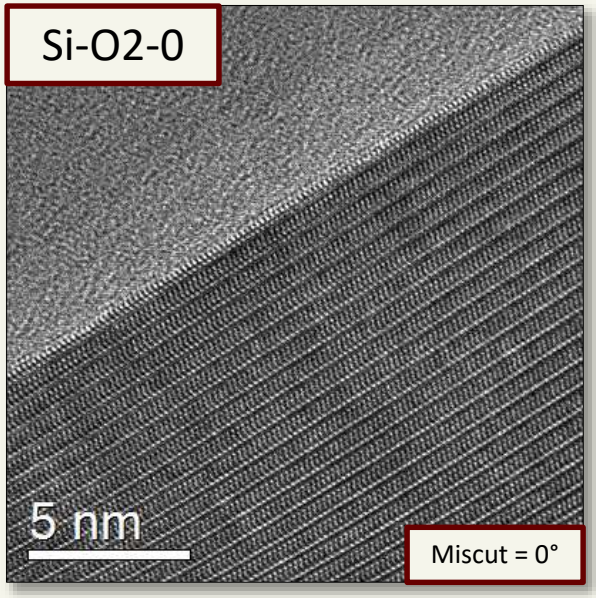
- 2 x 3 matrix aimed at comparing substrate orientation (and miscut) with processing conditions:
  - NO POA is for 2hr, all SiC substrates are n-type, SiO_2 ~60 nm thick

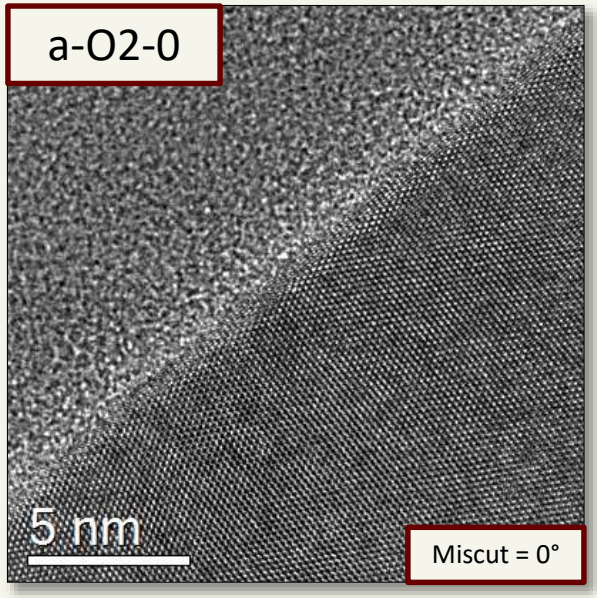
Sample Labels:	**Only oxidized**	**NO Post-annealed**
Si-face on-axis	Si-O_2-0	Si-N-0
Si-face miscut (4°)	Si-O_2-4	Si-N-4
a-face on-axis	a-O_2-0	a-N-0

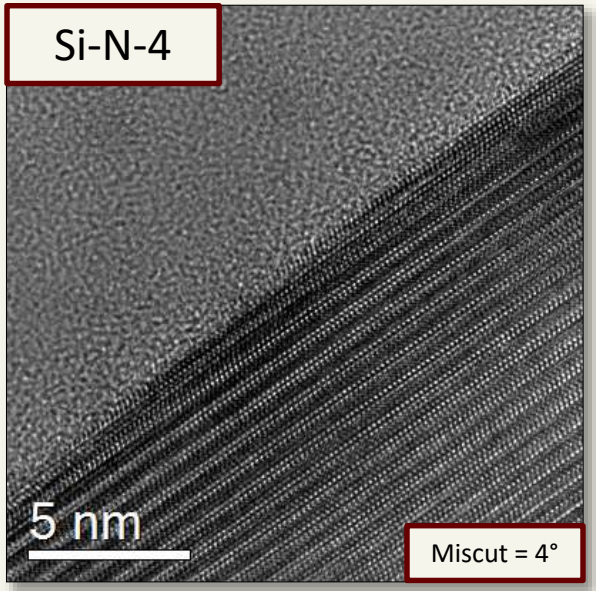


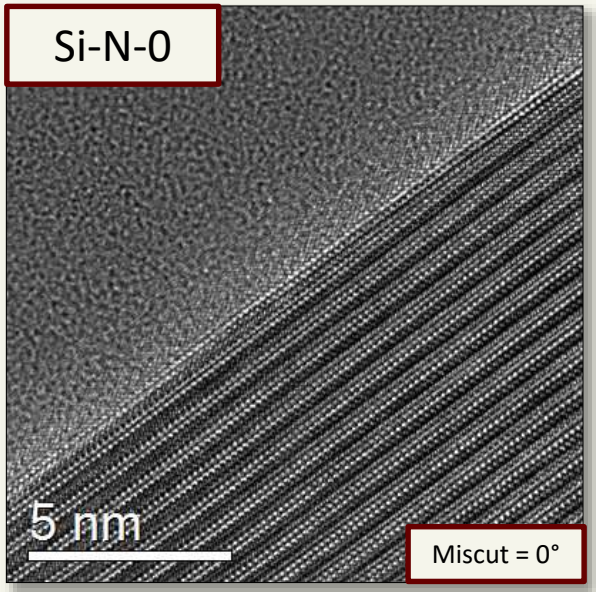
Si-face and *a*-face with and without NO annealing

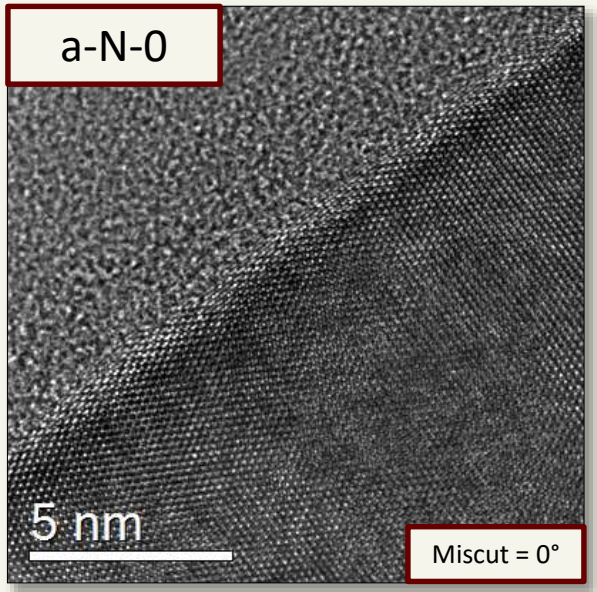




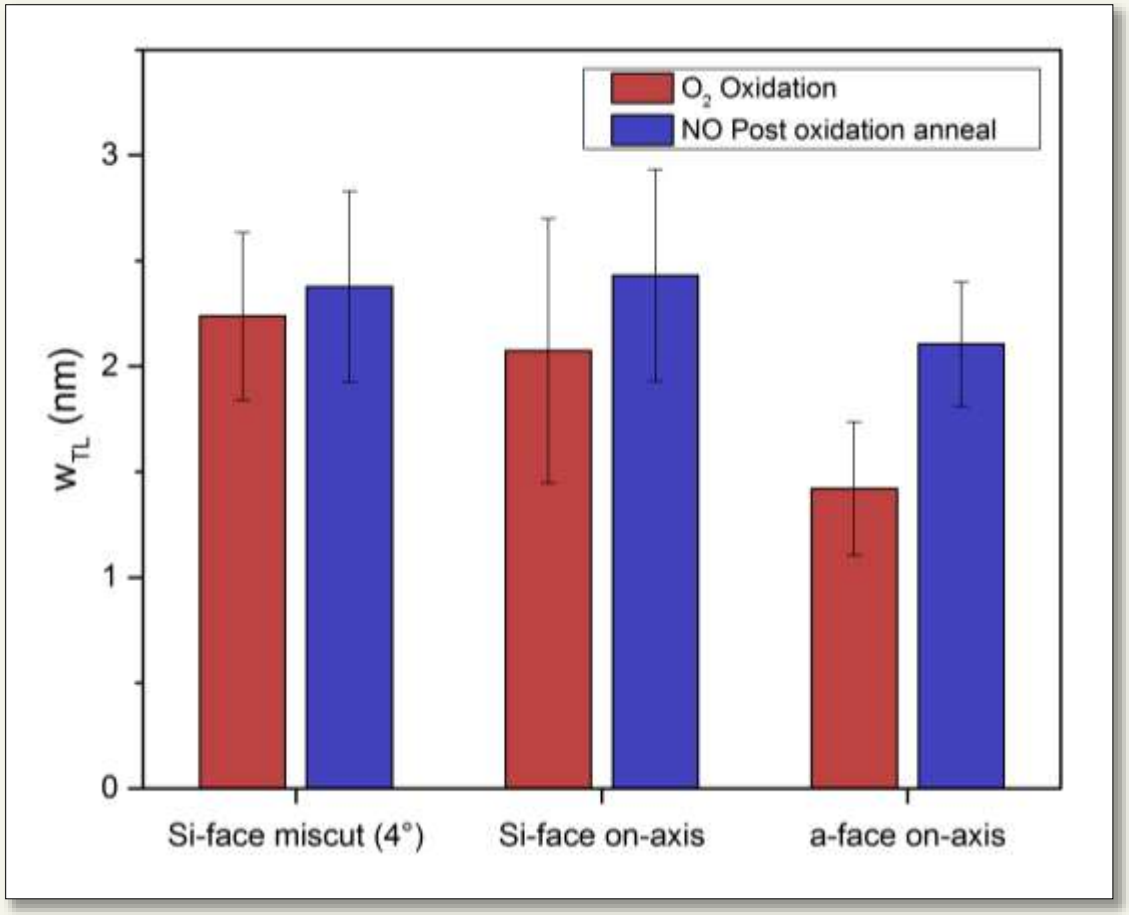








w_{TL} measurements



- Results from STEM EELS transition layer measurements show that w_{TL} values are similar
- w_{TL} in NO-annealed samples for these devices are actually slightly larger than the non-annealed
- a-face interfaces are the smallest, which does correspond with their higher mobilities (in NO)
  - 40 cm^2/V s for Si-face
  - 85 cm^2/V s for a-face

XPS DEPTH PROFILING

Etching experimental setup

- Developed by Grunthaner, Grunthaner, and Vasquez for use on Si/SiO_2 interfaces in the 1970s[1,2]
- Further refined by Fenner *et al.* in the 1980s[3]

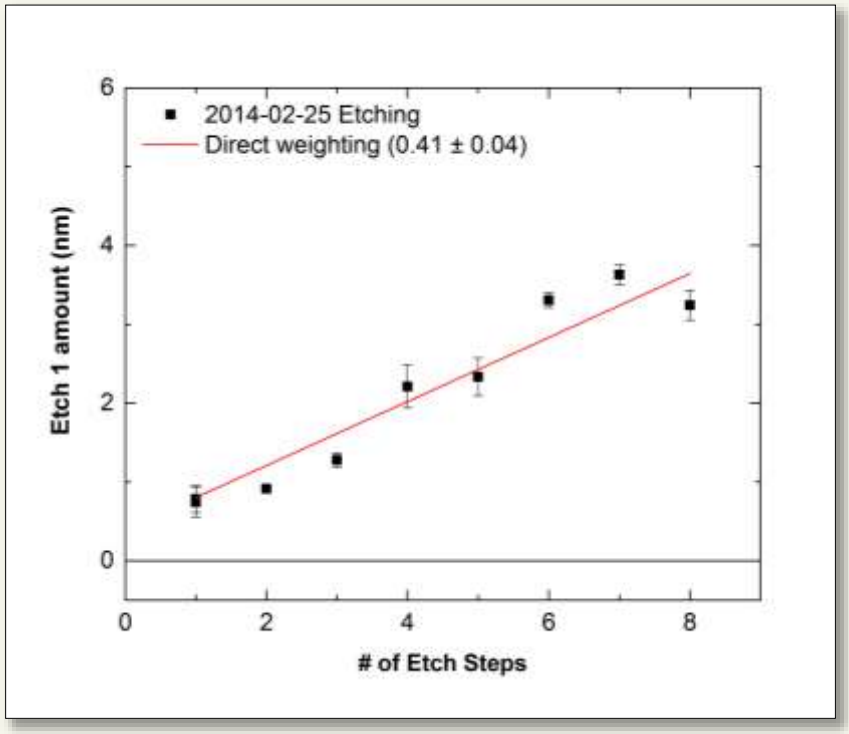
- Etchant solution is 10:1:1 ratio of $EtOH:H_2O$:49.5% HF (HPLC-grade)
- Manually pipette 25 µL drops in groups of 5 drops (each group is 1 "step")
- Dry sample using N_2 blow gun after each step

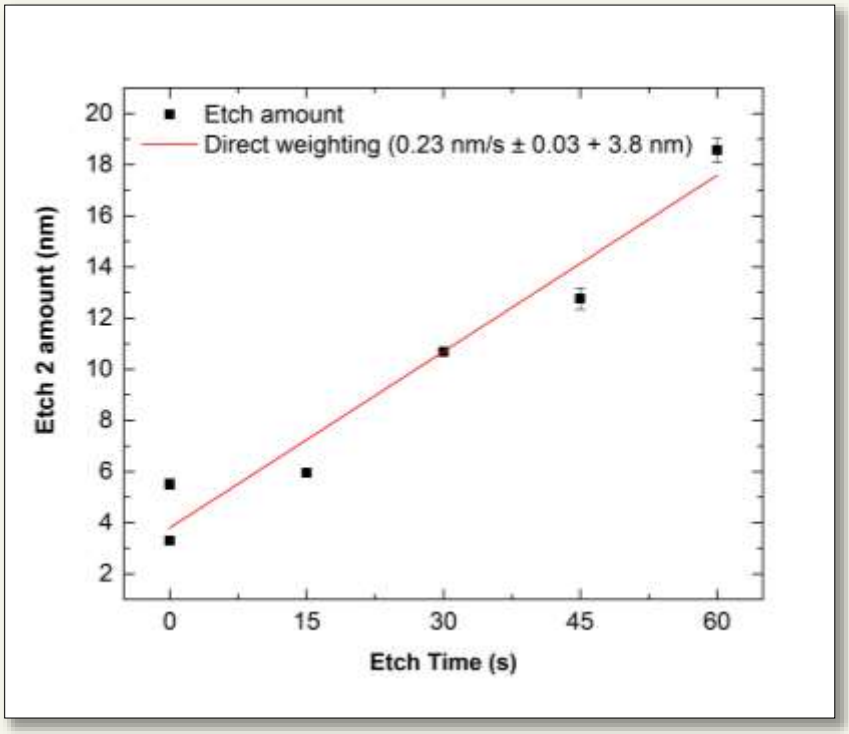
- Much more controllable, lower contamination, and less damaging than dip-etching or sputtering

- Controls explored:
  - Number of steps
  - Oxide type (wet or dry SiO_2 on Si)
  - Time etchant is left before drying
  - Time between etch steps

[1]F. J. Grunthaner, P. J. Grunthaner, et al., J. Vac. Sci. Technol., 16(5), 1443 (1979)
[2]R. P. Vasquez and F. J. Grunthaner, J. Appl. Phys., 52(5), 3509 (1981).
[3]D. B. Fenner, D. K. Biegelsen and R. D. Bringans, J. Appl. Phys., 66(1), 419 (1989).

Control via steps and time





"Short" exposure
(~2 seconds between steps)
Dry thermal oxide
0.4 nm removed per step

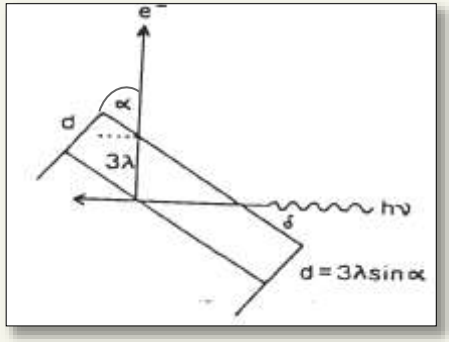
"Variable" exposure
(change time between steps)
Dry thermal oxide
0.2 nm removed per second

Sample overview

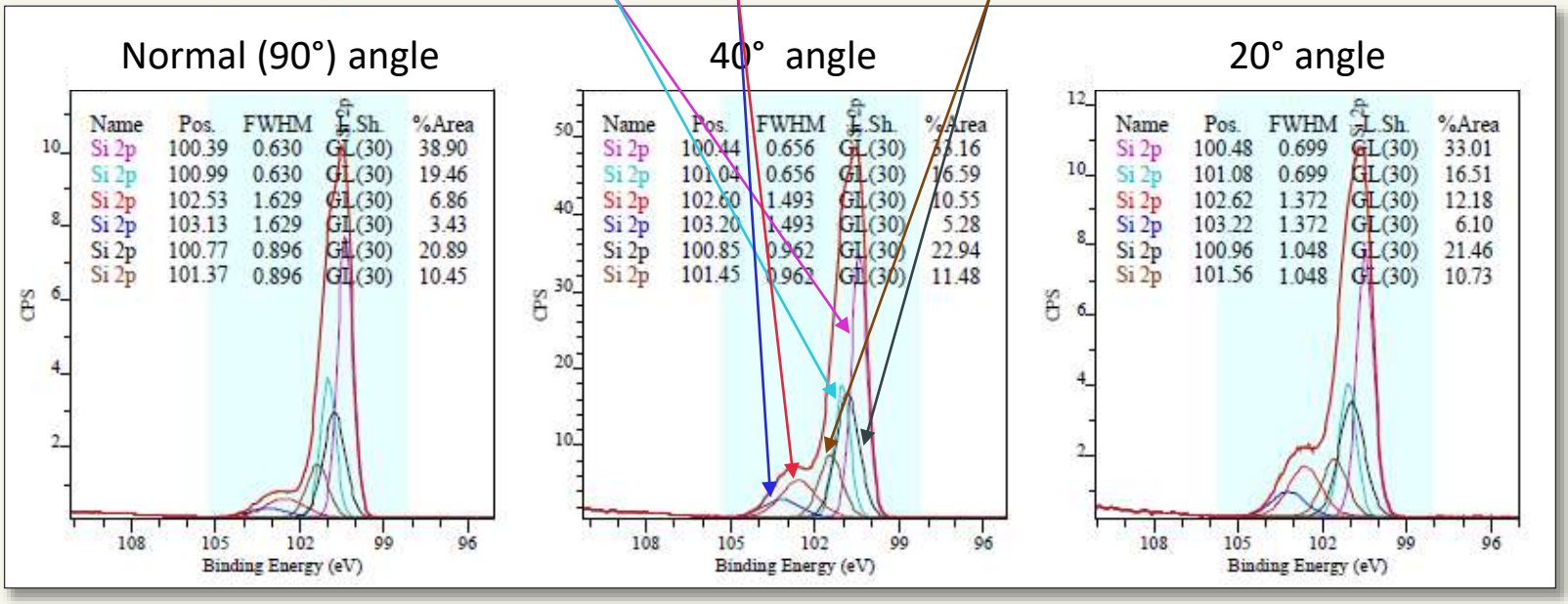
- 4 SiC/SiO_2 samples were provided by Rutgers
  - All are n-type with 10^{16} cm^{-3} doping
  - Two samples were just oxidized (labeled O1 and O2)
  - Two samples received 2hr NO post-oxidation anneal (labeled N1 and N2)
  - Starting oxide thicknesses were ~55nm

- Profiling:
  - O1 and N1 etched completely of SiO_2 with spin-etch technique
  - O2 etched to ~4nm thickness; N2 etched to ~2nm thickness
  - AR-XPS of Si-2*p*, N-1*s*, and C-1*s*

XPS Results – Si 2*p*



- Fit Si 2*p* with spin-orbit split components
  - Angle-resolved XPS allows us to probe different depths
  - Constrained fit by known physical phenomena to reduce spurious peak fits, i.e, $I_{2p1/2}:I_{2p3/2} = 1:2$
  - 3 components found: Substrate, oxide, and substrate surface/interface



Sample O1 – completely etched oxidized SiC sample

XPS Results – Si $2p\ ^{3}/_{2}$

- Looking at the peak position (binding energy) for each sample, we can see something interesting:

Sample	Substrate (I_o)	Oxide(I_o)	Substrate surface (I_s)
O1 – normal	102.5	102.5	100.8
O1 – 40°	102.6	102.6	100.9
O1 – 20°	102.6	102.6	101.0
N1 – normal	102.3	102.1	100.7
N1 – 40°	102.4	102.4	100.8
N1 – 20°	102.5	102.5	100.9
O2 – normal	103.1	103.1	100.7
O2 – 40°	103.2	103.2	100.7
O2 – 20°	103.2	103.2	100.9
N2 – normal	103.0	103.0	100.7
N2 – 40°	102.9	102.9	100.7
N2 – 20°	103.0	103.0	100.8

Completely etched

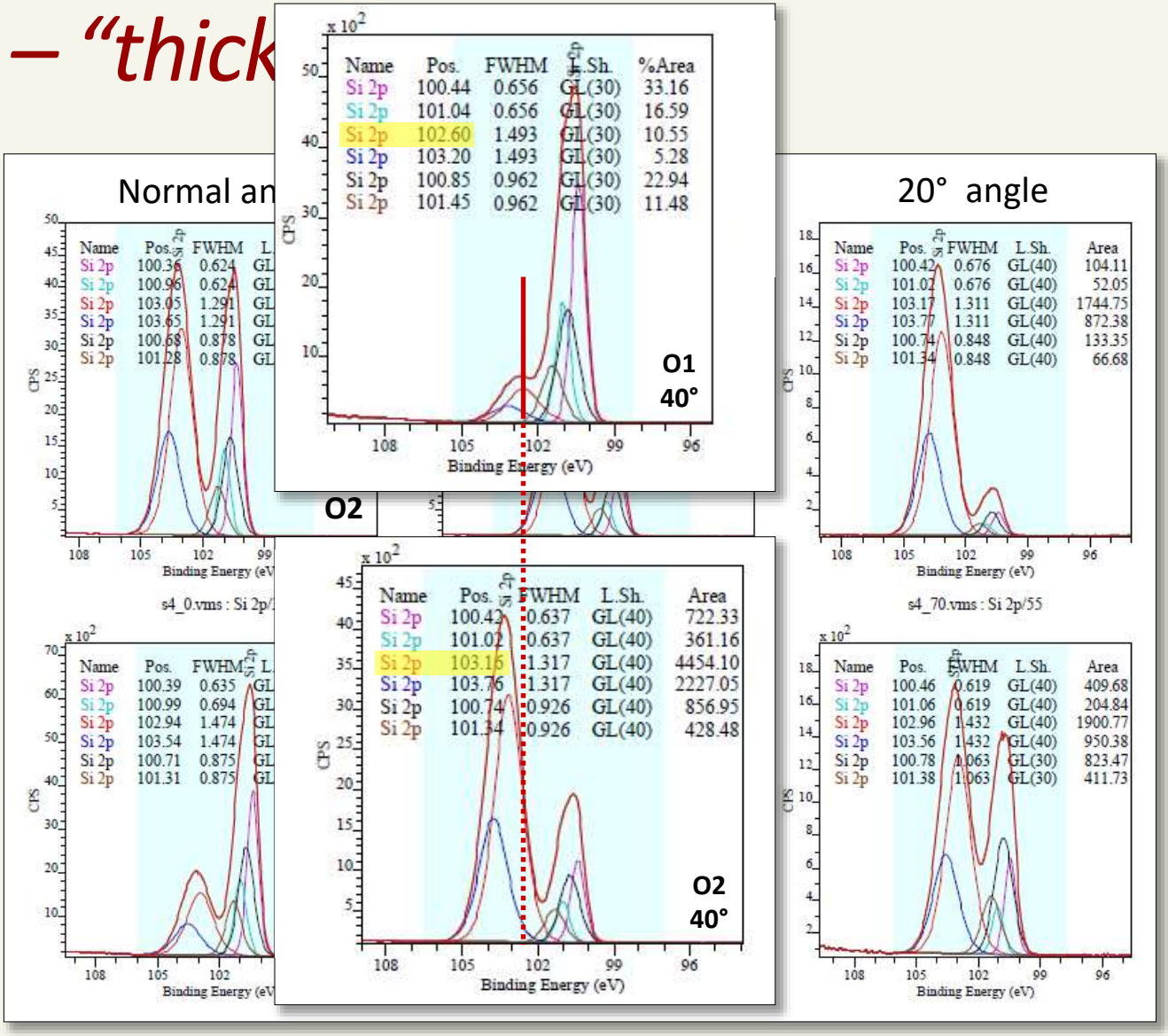
2 – 4 nm oxide layers

We can determine these samples were completely etched, and have reformed a "native oxide" that is at a lower binding energy

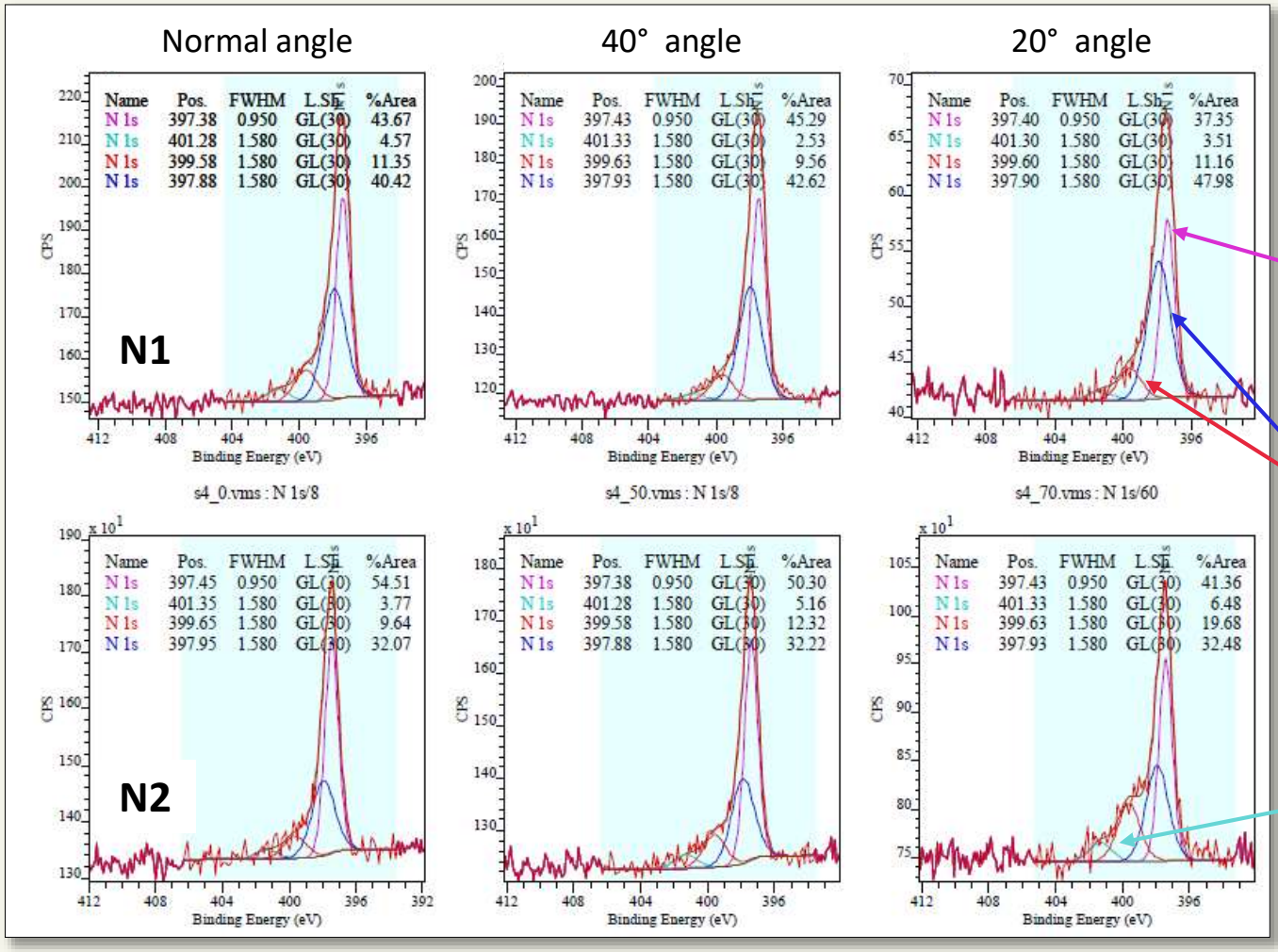
These samples are at the normal SiO_2 binding energy, so some of the true oxide remains

XPS – Si 2*p* – *"thick*

- No apparent influence of N in the Si 2*p*, but we might not expect to see it anyway due to the low concentration
- 2*p* signals for Si in samples with thicker oxide do not show any evidence of "suboxide" or "native" oxide states



XPS N 1*s*



- 4 components found in constrained fit:
  - Primary peak is consistent with silicon nitride-like bonding
  - Other peaks likely to be successively more oxygen bonding and/or carbon bonding
  - Additional component at higher energy[1]

[1]Y. Xu, L. C. Feldman, *et al.*, J. Appl. Phys., 115(3), 033502 (2014).

XPS N 1*s*

Completely etched

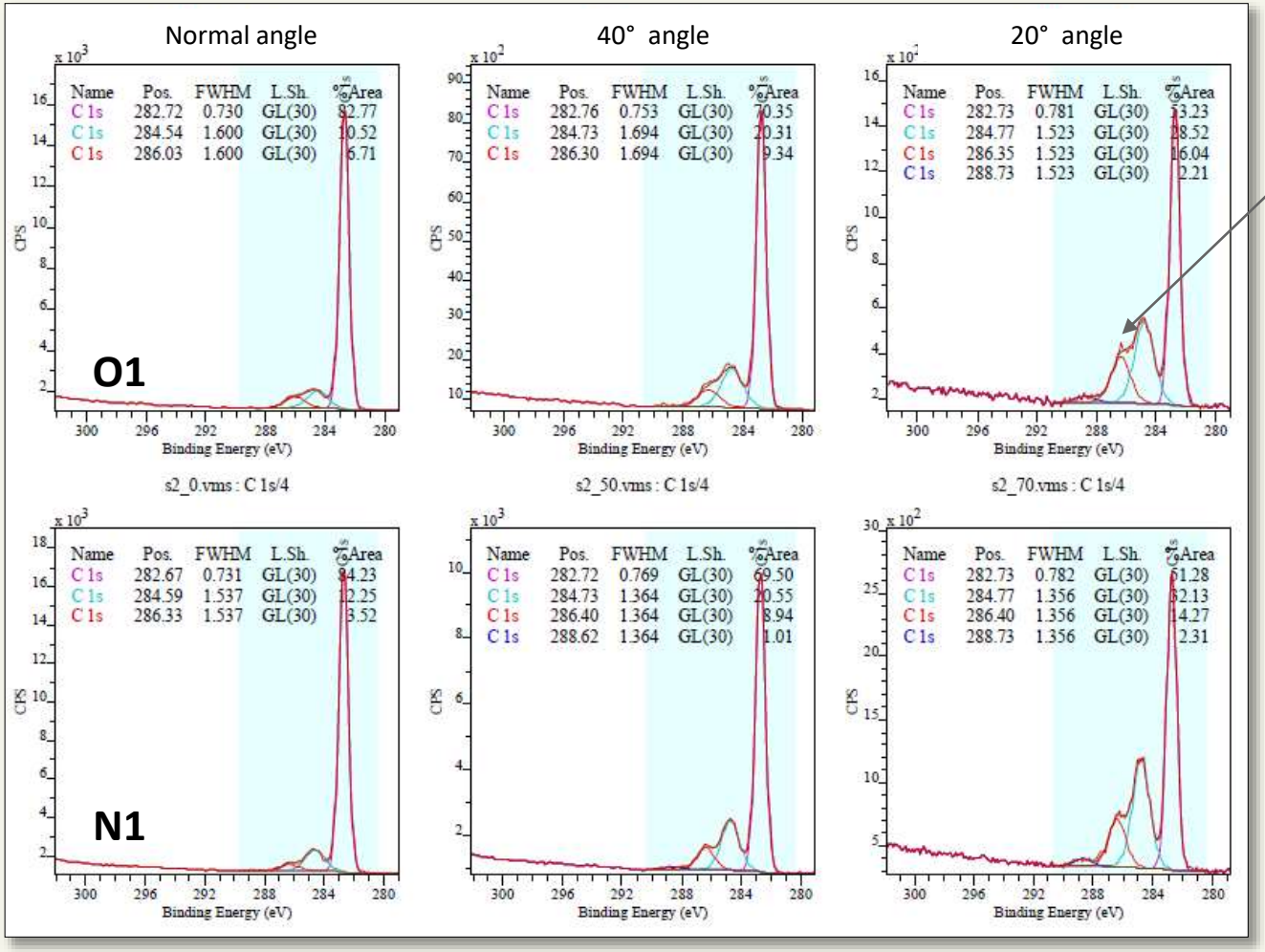
2 – 4 nm oxide layers

Elemental composition (peak area integration)				
Measurement	C 1s %	N 1s %	O 1s %	Si 2p %
N1 - normal	40.95	1.67	9.56	47.82
N1 – 40°	41.43	2.66	16.44	39.47
N1 – 20°	41.20	2.73	20.59	35.49
N2 – normal	29.92	1.01	21.80	47.28
N2 – 40°	33.59	1.37	29.46	35.58
N2 – 20°	36.28	1.45	33.57	28.70

- N content decreases when thick oxide is present, and is still present after all original oxide is etched off
- N is localized in SiC near interface (in agreement with paper from Rutgers[1])

[1]Y. Xu, L. C. Feldman, *et al.*, J. Appl. Phys., 115(3), 033502 (2014).

XPS C 1*s*



- Appears there is more C bonded to higher electronegativity atoms than we would expect from just contamination
- Possible C-O bonding at the interface
- Appears that NO anneal might reduce C-O peak (and perhaps C-O defect), but this needs more investigation

Summary

- The shift of the Si-$L_{2,3}$ edge is a good indicator of the width of the transition region in 4H SiC/SiO_2.
  - What physical change is occurring in the shifting region:
    - Variation in composition, strain, trap density, something else?
- NO post-anneal had been shown to decrease width of the transition region
  - Recent results suggest this may no longer be the case
- a-face samples have narrower transition region than Si-face.
- XPS indicates Si_3N_4-like N bonding at the interface.
- NO annealing reduces C-O signal in XPS possibly due to C-O defects.

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THANK YOU

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